APPARATUS AND METHOD FOR SPLIT TRANSISTOR MEMORY HAVING IMPROVED ENDURANCE

ABSTRACT OF THE DISCLOSURE

The present invention includes floating gate transistor structures used in non-volatile memory devices such as flash memory devices. In one embodiment, a system includes a CPU and a memory device including an array having memory cells having columnar structures and a floating gate structure interposed between the structures that is positioned closer to one of the structures. In another embodiment, a memory device includes an array having memory cells having adjacent FETs having source/drain regions and a common floating gate structure that is spaced apart from the source/drain region of one FET by a first distance, and spaced apart from the source/drain region of the opposing FET by a second distance. In still another embodiment, a memory device is formed by positioning columnar structures on a substrate, and interposing a floating gate between the structures that is closer to one of the structures.